# **DSP LOGIC BOARD**

## OVERVIEW

The DSP LOGIC BOARD takes a digital input from the A/D Converter on the Analog Input Board and performs all of the computations related to the measurement before it is displayed on the screen. This includes generating the digital reference sine wave, demodulating the signal, low-pass filtering the results, and offset and expanding the outputs. The internal oscillator sine output and Aux D/A outputs are generated on this board as well. The reference phase lock loop controls the clock of this board whenever the reference mode is external. These functions are implemented within a system comprised of five functional blocks: the Digital Signal Processor (DSP), the DAC Outputs, the Timing Signal Generator, the Reference Clock Generator and the I/O Interface. Through the use of highly efficient algorithms, the system is capable of real-time lock-in operation to 100 kHz with 24 dB/oct filtering on both X and Y as well as providing a synthesized analog sine output.

### DSP PROCESSOR

The SR830 utilizes a Motorola 24-bit DSP56001 digital signal processor (U501). The DSP is configured without external memory. The lock-in algorithms run entirely within the internal program and data memory of the DSP itself. The Host processor bus is connected to the main CPU Board via the I/O Interface on the DSP Logic Board. The 80C186 processor on the CPU Board acts as the "host" processor to the DSP. DSP firmware and commands are downloaded from the CPU Board to invoke different operating modes. The DSP also has two dedicated serial ports: one for receiving, and one for transmitting.

#### REFERENCE CLOCK SOURCE

The clock to the DSP is derived from the timing generator. U120, U121 and U122 are gates which select the clock source for the entire digital board.

When the reference mode is internal, the 30.208 MHz crystal (U111) is used. The A/D inputs and D/A outputs run with a 256 kHz cycle and the DSP performs 59 instructions each cycle (each instruction takes two clocks). The crystal

also sets the internal reference frequency accuracy.

When the reference mode is external, the VCO (voltage controlled oscillator, U110) is used as the system clock. The VCO nominally runs at 30 MHz as well. U105 is a phase comparator. The external reference input, discriminated by U103 (or TTL buffered through U104D) is one of the inputs to the phase comparator. The other input is the internal reference. The DSP always synthesizes a sine wave at the reference frequency. This is the Sine Output. This sine output is discriminated by U209 into a TTL square wave (TTL Sync Out) and is the other input to the phase comparator. The phase lock loop then controls the VCO which is the clock to the DSP. This in turn changes the sine output frequency to maintain frequency lock with the external reference. The DSP is constantly getting external frequency information from the host (based upon counter U622) which allows the DSP to synthesize nearly the correct reference frequency assuming a 30 MHz clock. This keeps the VCO within range at all frequencies.

## TIMING GENERATOR

All timing signals for the DSP and Analog boards are derived from the system clock by PALs (U601-604). These PALs generate the clocks for the DACs and A/D converter, the multiplexing signals for the Aux inputs and outputs, etc.

## SERIAL CHANNELS

There are two serial data streams from the A/D converter on the Analog Input board which need to be received by the DSP. The digitized input signal is received directly via the DSP's serial input port. The Aux A/D input data is shifted into a pair of serial-to-parallel registers (U502 and U503) and is read via the DSP data bus. Each A/D input channel provides a new sample every 4 µs.

There are two dual-channel D/A converters on this board for a total of four D/A output channels. Each output channel provides a new output every 4  $\mu$ s. This means that 4 output values must be written by the DSP each 4  $\mu$ s cycle. The DSP writes to one channel of each D/A converter via its serial