SERVICE REQUESTS (SRQ)

A GPIB service request (SRQ) will be generated whenever a bit in both the Serial Poll Status byte AND Serial Poll Enable register is set. Use ⁎SRE to set bits in the Serial Poll Enable register. A service request is only generated when an enabled Serial Poll Status bit becomes set (changes from 0 to 1). An enabled status bit which becomes set and remains set will generate a single SRQ. If another service request from the same status bit is desired, the requesting status bit must first be cleared. In the case of the ERR, LIA and ESB bits, this means clearing the enabled bits in the ERR, LIA and ESB status bytes (by reading them). Multiple enabled bits in these status bytes will generate a single SRQ. Another SRQ (from ERR, LIA or ESB) can only be generated after clearing the ERR, LIA or ESB bits in the Serial Poll status byte. To clear these bits, ALL enabled bits in the ERR, LIA or ESB status bytes must be cleared.

The controller should respond to the SRQ by performing a serial poll to read the Serial Poll status byte to determine the requesting status bit. Bit 6 (SRQ) will be reset by the serial poll.

For example, to generate a service request when a RESRV overload occurs, bit 0 in the LIA Status Enable register needs to be set (LIAE 0,1 command) and bit 3 in the Serial Poll Enable register must be set (⁎SRE 3,1 command). When a reserve overload occurs, bit 0 in the LIA Status byte is set. Since bit 0 in the LIA Status byte AND Enable register is set, this ALSO sets bit 3 (LIA) in the Serial Poll Status byte. SInce bit 3 in the Serial Poll Status byte AND Enable register is set, an SRQ is generated. Bit 6 (SRQ) in the Serial Poll Status byte is set. Further RESRV overloads will not generate another SRQ until the RESRV overload status bit is cleared. The RESRV status bit is cleared by reading the LIA Status byte (with LIAS?). Presumably, the controller is alerted to the overload via the SRQ, performs a serial poll to clear the SRQ, does something to try to remedy the situation (change gain, experimental parameters, etc.) and then clears the RESRV status bit by reading the LIA status register. A subsequent RESRV overload will then generate another SRQ.

STANDARD EVENT STATUS BYTE

bit	name	usage
0	INP	Set on input queue overflow (too many commands received at once, queues cleared).
1	Unused	
2	QRY	Set on output queue overflow (too many responses waiting to be transmitted, queues cleared).
3	Unused	
4	EXE	Set when a command can not execute correctly or a parameter is out of range.
5	CMD	Set when an illegal command is received.
6	URQ	Set by any key press or knob rotation.
7	PON	Set by power-on.

The bits in this register remain set until cleared by reading them or by the ⁎CLS command.