SR-830 DSP Lock-In Amplifier Specifications

SR810 and SR830 Specifications

Signal Channel

Voltage inputs	Single-ended or differential
Sensitivity	2 nV to 1 V
Current input	10^6 or 10^8 V/A
Input impedance	
Voltage	10 MΩ + 25 pF, AC or DC coupled
Current	1 kΩ to virtual ground
Gain accuracy	±1 % (±0.2 % typ.)
Noise (typ.)	6 nV/√Hz at 1 kHz 0.13 pA/√Hz at 1 kHz (10^6 V/A) 0.013 pA/√Hz at 100 Hz (10^8 V/A)
Line filters	50/60 Hz and 100/120 Hz (Q = 4)
CMRR	100 dB to 10 kHz, decreasing by 6 dB/oct above 10 kHz
Dynamic reserve	>100 dB (without prefilters)
Stability	<5 ppm/°C

Reference Channel

Frequency range	0.001 Hz to 102.4 kHz
Reference input	TTL or sine (400 mVpp min.)
Input impedance	1 MΩ, 25 pF
Phase resolution	0.01° front panel, 0.008° through computer interfaces
Absolute phase error	<1°
Relative phase error	<0.001°
Orthogonality	90° ± 0.001°
Phase noise	
Internal ref.	Synthesized, <0.0001° rms at 1 kHz
External ref.	0.005° rms at 1 kHz (100 ms time constant, 12 dB/oct)
Phase drift	<0.01°/°C below 10 kHz, <0.1°/°C above 10 kHz
Harmonic detection	2F, 3F, ... nF to 102 kHz (n < 19,999)
Acquisition time	(2 cycles + 5 ms) or 40 ms, whichever is larger

Demodulator

Stability	Digital outputs and display: no drift Analog outputs: <5 ppm/°C for all dynamic reserve settings
Harmonic rejection	–90 dB
Time constants	10 µs to 30 ks (6, 12, 18, 24 dB/oct rolloff). Synchronous filters available below 200 Hz.

Internal Oscillator

Range	1 mHz to 102 kHz
Frequency accuracy	25 ppm + 30 µHz
Frequency resolution	4½ digits or 0.1 mHz, whichever is greater
Distortion	–80 dBc (f <10 kHz), –70 dBc (f >10 kHz) @ 1 Vrms amplitude
Amplitude	0.004 to 5 Vrms into 10 kΩ (2 mV resolution), 50 Ω output impedance, 50 mA maximum current into 50 Ω
Amplitude accuracy	1 %
Amplitude stability	50 ppm/°C
Outputs	Sine, TTL (When using an external reference, both outputs are phase locked to the external reference.)

Displays

Channel 1	4½-digit LED display with 40-segment LED bar graph. X, R, X-noise, Aux 1 or Aux 2. The display can also be any of these quantities divided by Aux 1 or Aux 2.
Channel 2 (SR830)	4½-digit LED display with 40-segment LED bar graph. Y, θ, Y-noise, Aux 3 or Aux 4. The display can also be any of these quantities divided by Aux 3 or Aux 4.
Offset	X, Y, R can be offset up to ±105 % of full scale.
Expand	X, Y, R can be expanded by 10× or 100×.
Reference	4½-digit LED display

Inputs and Outputs

CH1 output	X, R, X-noise, Aux 1 or Aux 2, (±10 V), updated at 512 Hz
CH2 output (SR830)	Y, θ, Y-noise, Aux 3 or Aux 4, (±10 V), updated at 512 Hz
X, Y outputs (rear panel)	In-phase and quadrature components (±10 V), updated at 256 kHz.
Aux. A/D inputs	4 BNC inputs, 16-bit, ±10 V, 1 mV resolution, sampled at 512 Hz
Aux. D/A outputs	4 BNC outputs, 16-bit, ±10 V, 1 mV resolution
Sine out	Internal oscillator analog output
TTL out	Internal oscillator TTL output
Data buffer	The SR810 has an 8k point buffer. The SR830 has two 16k point buffers. Data is recorded at rates to 512 Hz and read through the computer interfaces.
Trigger in (TTL)	Trigger synchronizes data recording
Remote preamp	Provides power to the optional SR550, SR552 and SR554 preamps

General

Interfaces	IEEE-488.2 and RS-232 interfaces standard. All instrument functions can be controlled and read through IEEE-488.2 or RS-232 interfaces.
Power	40 W, 100/120/220/240 VAC, 50/60 Hz
Dimensions	17" × 5.25" × 19.5" (WHD)
Weight	23 lbs.
Warranty	One year parts and labor on defects in materials and workmanship

SRS Stanford Research Systems

phone: (408)744-9040
www.thinkSRS.com