Individual Names (Bit Patterns) Cannot be Shared

Note that
- **using** some "memory" **addresses for I/O**
- **implies NOT using those addresses for memory**.

This constraint can be an issue when memory addresses are few (16-bit or less).

In the LC-3 ISA,
- addresses xFE00-xFFFF are used for I/O
- (1/128th of memory).

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Keyboard and Display are Memory-Mapped in LC-3

Keyboard and display registers are mapped as follows:*

xFE00 KBSR
xFE02 KBDR
xFE04 DSR
xFE06 DDR

Other addresses are reserved for future use.

Let's take a look at how I/O is implemented.

*Why every other address? P&P defined a variation on LC-3 for seniors to implement; LC-3b has byte-addressable memory.

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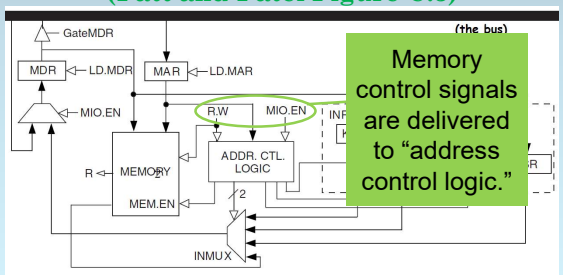
P&P Appendix C Describes I/O Memory Mapping

(Patt and Patel Figure C.3)



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Keyboard and Display are Memory-Mapped in LC-3

Based on MAR and these control signals, the **address control logic controls**:
- **memory enable** (chip select) signal actually delivered to the memory,
- **load control for DDR**,* and
- **INMUX select** lines, which determines whether memory, KBSR, KBDR, or DSR writes the load result to MDR.

*And for KBSR and DSR, but we'll explain why later.

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